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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,467	03/11/2004	Brian T. Lewis	ITL.1534US (P18671)	7703
21906 7590 09/04/2007 TROP PRUNER & HU, PC 1616 S. VOSS ROAD, SUITE 750 HOUSTON, TX 77057-2631			EXAMINER CHAVIS, JOHN Q	
			ART UNIT	PAPER NUMBER
			2193	
			MAIL DATE	DELIVERY MODE
			09/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/799,467

Applicant(s)

LEWIS ET AL.

Examiner

John Chavis

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2193

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-56 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-56 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application
- ☐ Other: _____

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Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Crelier and further in view of the applicant's choice of providing for garbage collection and optimizations to enable direct invocations of methods and the applicant's choice of memory to utilize to enable faster, more efficient processing.

What is claimed is:

1. A method comprising: relocating a compiled code block associated with a software application;

wherein said relocating is performed responsive to hardware event information gathered during current execution of the software application;

and wherein said relocating is performed during current execution

Crelier

Crelier does not specifically indicate that code is relocated; however, he specifies that when code is relocated, fix-ups are required, see col. 3 lines 27-35. Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to enable relocations in Crelier's when required to compensate for garbage collection, optimizations, to enable direct invocations of methods, etc. (see col. 12 lines 41-56) in which code is relocated to improve memory consumption or execution speed (even if it just a little), see col. 6 lines 55-66.

Optimizations are performed responsive to the specific hardware system utilized in which the event is to improve processing speed based on the specific system, see col. 3 lines 6-16.

Note that relocations may occur at runtime (during current execution), see

of the software application.

2. The method of claim 1, further comprising: selecting the compiled code block responsive to occurrence of a trigger condition during current execution of the software application.

3. The method of claim 2, wherein: the hardware event information indicates that the trigger condition has occurred during current execution of the software program.

4. The method of claim 2, wherein: the trigger condition is a threshold number of hardware performance events.

5. The method of claim 4, wherein: the trigger condition is a threshold number of instruction miss events.

6. The method of claim 2, wherein: the trigger condition is a set of hardware criteria.

7. The method of claim 2, wherein: the trigger condition is a set of hardware and software criteria.

col. 3 lines 27-35.

See the rejection of claim 1.

See the rejection of claim 1.

This feature is considered a typical reason for optimizations in order to determine when to optimize. Therefore, It would have been obvious to a person having ordinary skill in the art at the time of the invention to utilize the feature in Crelier's system for the same reason.

" " " "

" " " "

" " " ". It was further well known in the art at the time of the Invention that optimizations can be based on a variety of parameters, such as the hardware information provided above and to provide optimizations for code that is executed more frequently or to improve execution of repetitive functions, such as loops, etc. Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to provide optimizations in Crelier's system for the same reasons

8. The method of claim 1, further comprising: selecting the compiled code block based on the compiled code block's resource utilization during current execution of the software application.

9. The method of claim 8, wherein: the hardware event information reflects the compiled code block's resource utilization during current execution of the software program.

10. The method of claim 9, wherein: the hardware event information further reflects the number of executed method calls performed by the compiled code block.

11. The method of claim 9, wherein: the hardware event information further reflects the number of times the compiled code block has been called during execution of the software program.

12. The method of claim 9, wherein: standard the hardware event information further reflects the number of execution cycles consumed during execution of the compiled code block.

13. The method of claim 1, further comprising: relocating a virtual method table associated with the software application during current execution of the software application.

14. The method of claim 13,

to improve processing, storage and execution speed.

" " " "

" " " "

See the rejection of claim 9 in view of claim 4.

" " " "

" " " " These are conditions known in the art to affect execution speed.

See the reference above to optimizing storage utilizations.

See the rejections of claims 5-7.

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wherein: said hardware event information includes data miss information.

15. The method of claim 1, wherein: said relocating is performed on as-needed basis independent of garbage collection.

See the optimization feature above.

16. The method of claim 1, wherein said relocating further comprises: moving the compiled code block to a new location within a code region;

See the rejections above in view of col. 12 lines 41-56.

and patching address references in the code region to reflect the new location of the compiled code block.

" " " "

17. The method of claim 16, wherein: patching address references further comprises patching address references such that invocation of the relocated compiled code does not generate a trap.

" " " "

18. The method of claim 16, further comprising: patching a call stack to reflect the new location.

See col. 11 lines 36-41.

19. The method of claim 16, further comprising: patching a virtual method table to reflect the new location.

This feature is considered inherent via col. 4 lines 28-35.

In reference to claims 20-21, 28, see the rejection of claim 1.

The features of claim 22 are taught via claim 13.

As per claims 23-24, see the rejection of claim 3.

In reference to claim 25, see the rejection of claim 4.

The features of claims 26-27 are taught via claim 5.

As per claims 29-31, see the rejection of claim 7. Crelier does not specifically mention a history and a graph; however, the feature would have been obvious to a person having ordinary skill in the art at the time of the invention to provide such features in Crelier's system to provide indications of relocation information to enable visual representations of the optimizations.

See the rejection of claim 16 in view of claim 32.

In reference to claim 33, 52, see the rejection of claim 16 in view of claim 9. furthermore, the type of memory utilized does not create a different system. Therefore, although Crelier does not specifically indicate the type of memory utilized, it would have been obvious to a person having ordinary skill in the art at the time of the invention to utilize the newer types of memory in an old system, such as Crelier's, for their speed and versatility features.

As per claims 34-48, see the rejection of claim 33 in view of claim 7 in view of claim 5.

In reference to claims 53-56, see the rejection of claim 16 in view of claims 9 and 5-7.

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Chavis whose telephone number is (571) 272-3720. The examiner can normally be reached on M-F, 9:00am-5:30pm, EST.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JC



John Chavis
Primary Examiner AU-2193